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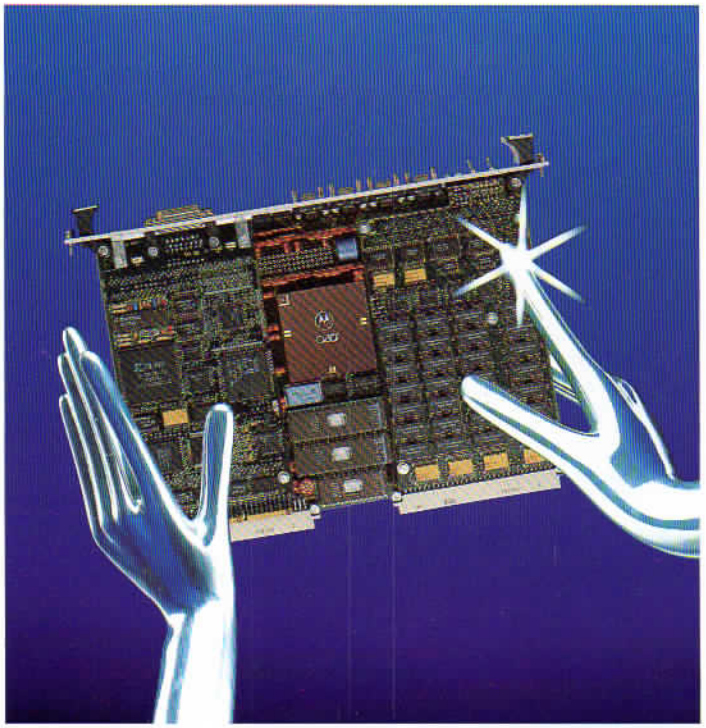
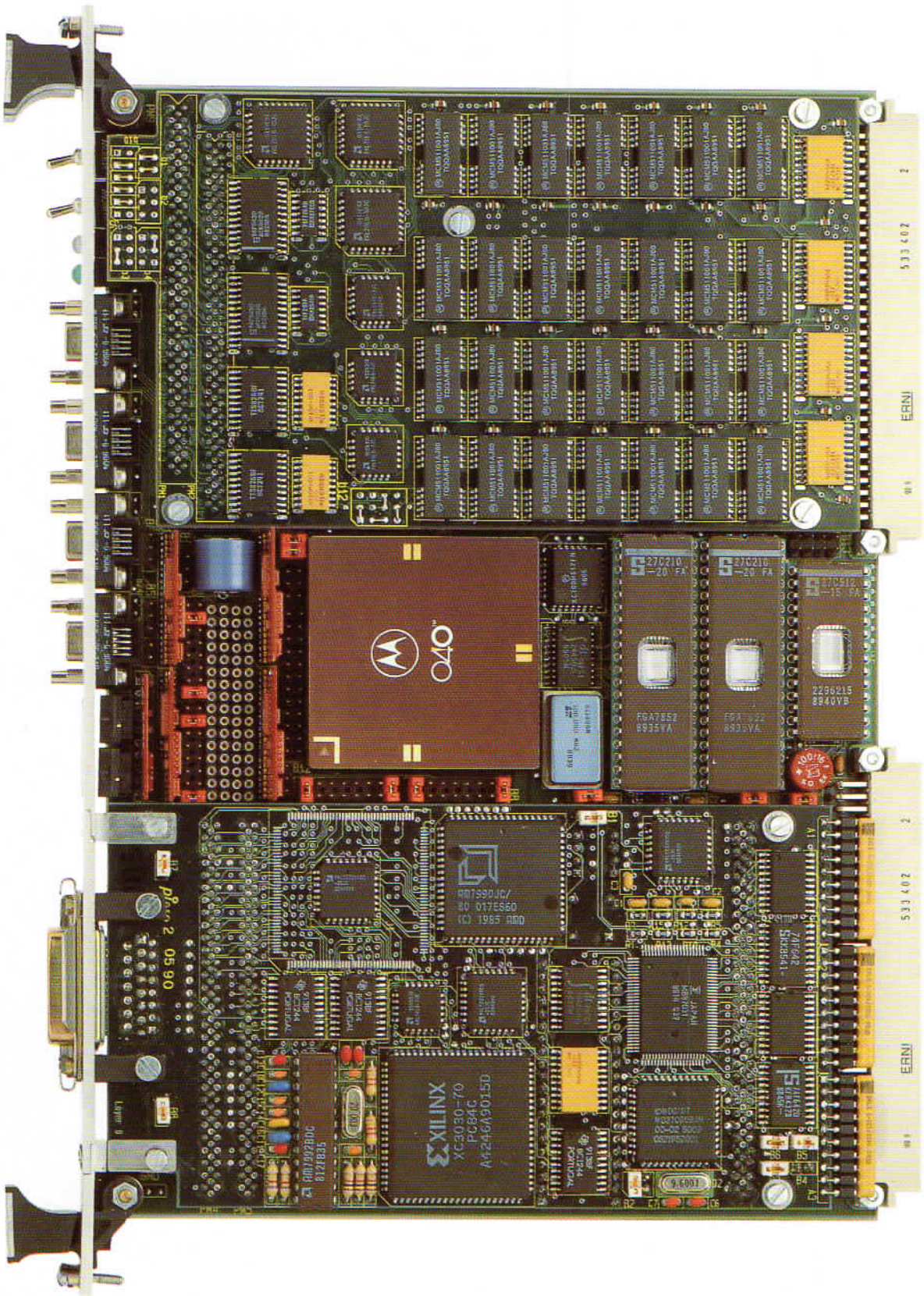


System 68000 VME
SYS68K/CPU-40
SYS68K/CPU-41

High Performance Multi-Purpose 68040 Board with Shared Memory, DMA and FLXibus

VME/PLUS™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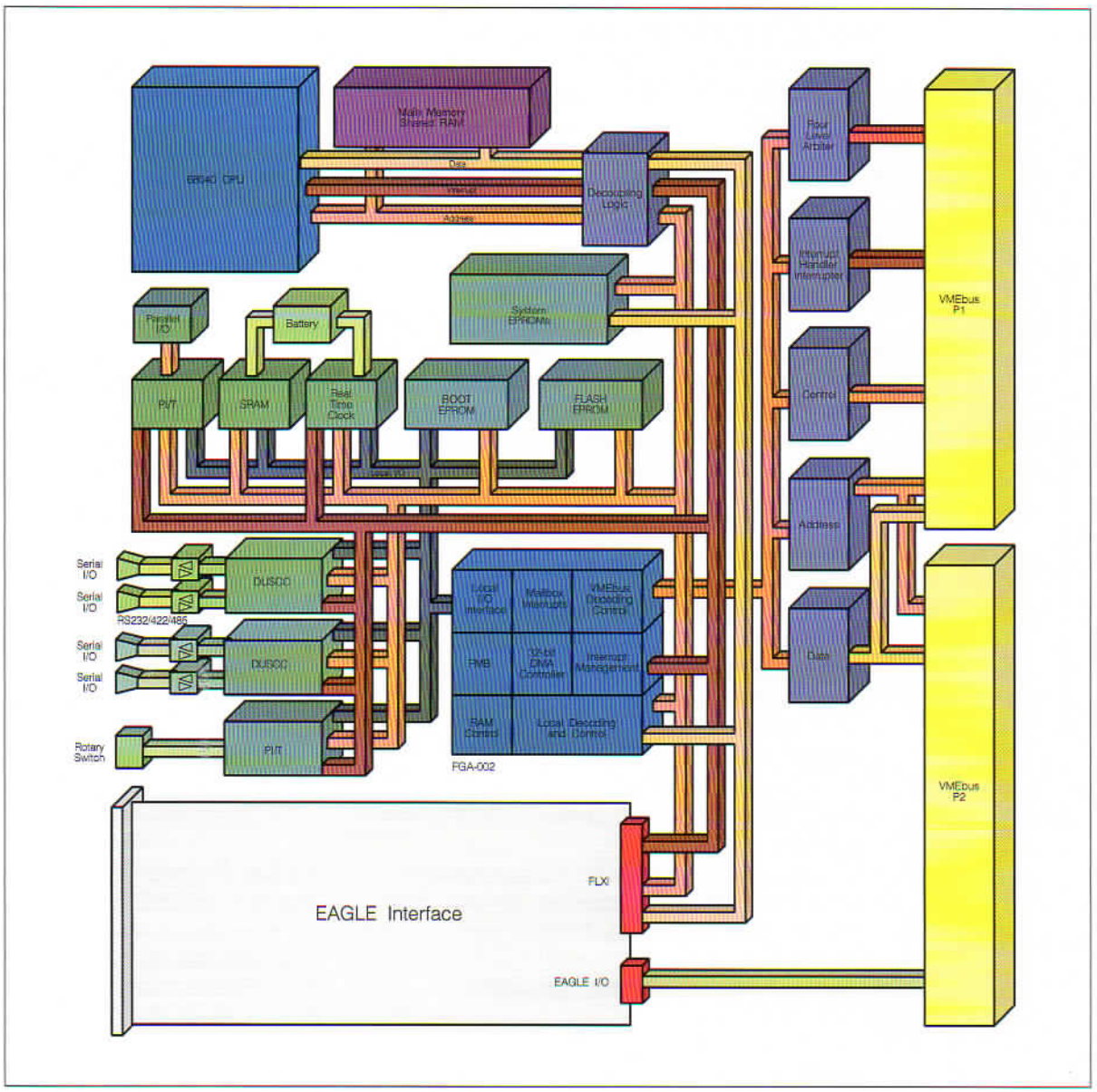
General Description

The SYS68K/CPU-40 and the SYS68K/CPU-41 are high performance CPU-boards based on the 68040 microprocessor and the VMEbus. The boards incorporate a modular I/O subsystem which provides a high degree of flexibility for a wide variety of applications. The CPU-40 and the CPU-41 can be used with or without an I/O subsystem module (EAGLE module).
All of the EAGLE modules offered by FORCE COMPUTERS are fully compatible with the CPU-40 and the CPU-41. The CPU-40 is optionally available with 4, 16 or 32 Mbyte shared DRAM options, all with byte parity. The CPU-41 is optionally available with 4 or 8 Mbyte SRAM. The CPU-40 and the CPU-41 family design utilizes all of the features of the powerful FORCE FGA-002 VMEbus gate array. Among its features is a 32-bit DMA controller that supports local (shared) memory, VMEbus and I/O data transfers for maximum performance together with parallel real-time operation and responsiveness.

Block Diagram of the SYS68K/CPU-40 and the SYS68K/CPU-41



The EAGLE modules are installed on the CPU-40 and the CPU-41 via FLXibus (FORCE Local eXpansion interface). FLXi provides a full 32-bit interface between the base board and the EAGLE module I/O subsystem and supports a broad range of powerful I/O options.
Four multi-protocol serial I/O channels, a parallel I/O channel and a Real-Time Clock with on-board battery back-up are installed on the base board which, in combination with EAGLE modules, make these CPUs true single board computers.

A broad range of operating systems and kernels is available for the CPU-40 and the CPU-41. Additionally, the VMEPROM Real-Time Kernel/ debug monitor is provided with the board at no extra cost, ensuring that the board is supplied ready to use.

Features of the SYS68K/CPU-40 and CPU-41

- 68040 microprocessor @ 25.0 MHz
- Shared DRAM (CPU-40):
  4, 16 or 32 Mbyte with byte parity
- Shared SRAM (CPU-41): 4 or 8 Mbyte
- Full support of the burst fill mode of the 68040
- High speed 32-bit DMA controller (FGA-002) for data transfers to/from the shared RAM, the VMEbus and EAGLE modules.
- Two system EPROM sockets supporting 40-pin devices. Access from the 68040 with a 32-bit data path.
- One boot EPROM for local booting, initialization of the I/O chips and configuration of the FGA-002.
- 128 Kbyte SRAM with on-board battery back-up and/or +5V STDBY from VMEbus.
- 128 Kbyte Flash EPROM with on-board programming support.
- FLXi interface for installation of one EAGLE module.
- Four Serial I/O interfaces, configurable as RS232/RS422/RS485, available on the front panel.
- 8-bit parallel interface with 4-bit handshake.
- Real-Time Clock with calendar, on-board battery back-up and/or +5V STDBY from VMEbus.
- Two 24-bit timers with 5-bit prescaler.
- One 8-bit timer.
- Full 32-bit VMEbus master/slave interface, supporting the following data transfer types:
  – A32, A24, A16:D8, D16, D32 - Master
  – A32, A24:D8, D16, D32 - Slave
  – UAT, RMW, ADO
- FORCE Message Broadcast (FMB), two channels.
- Four level VMEbus arbiter.
- SYSCLK driver.
- VMEbus interrupter (IR 1-7).
- VMEbus interrupt handler (IH 1-7).
- Support for ACFAIL and SYSFAIL.
- Bus time-out counters for local and VMEbus access.
- VMEPROM, Real-Time Multitasking Kernel with monitor, file manager and debugger.

1. Hardware Description

1.1 The 68040 Microprocessor

The 68040 integrates a 68030 microprocessor superset, a 68881 compatible concurrent floating point core, separate 4 Kbyte instruction and data caches and a dual paged memory management unit on one VLSI device.
The 68040 is a full 32-bit implementation of the 68000 architecture, with a high speed 32-bit data path, instruction pipeline, and bus interface. The implementation of the 68040 has been optimized to minimize instruction execution time for compiler generated code.

Features of the 68040 at 25 MHz

- 19 MIPS sustained Integer Unit
- 3.6 MFLOPS concurrent Floating Point Unit
- Flexible high bandwidth synchronous bus
- 68020/68030 compatible integer unit
- 68881/68882 compatible floating-point unit
- Independent data and instruction memory management units
- 4 Kbyte on-chip data cache
- 4 Kbyte on-chip instruction cache
- 4 Gbyte addressing range
- Upward user object code compatible with the 68020/68030 and 68881/68882

1.2 The Shared Main Memory

The CPU-40 and the CPU-41 designs use memory modules for maximum flexibility of memory type and size. All modules provide memory that is accessible from the 68040 microprocessor, the local FLXibus and the VMEbus. The CPU-40 provides the user with DRAM and the CPU-41 with SRAM options.

1.2.1 The Shared DRAM

The main memory area of the CPU-40 is installed on a DRAM memory module populated with 1 Mbit or 4 Mbit devices to provide 4, 16 or 32 Mbyte of main memory. The memory module contains all the memory decoding logic, DRAM control logic, refresh generation, byte parity generation and checking, and address multiplexers/drivers.

1.2.2 The Shared SRAM

The main memory area of the CPU-41 is installed on an SRAM memory module populated with 1 Mbit devices to provide 4 Mbyte or 8 Mbyte of main memory. The memory module contains all the memory decoding logic, SRAM control logic and multiplexers/drivers. The SRAM can be battery backed via the +5V STDBY line of the VMEbus enabling full data retention during power down and/or power failures. With this feature, the CPU-41 is particularly suited for industrial applications.

1.2.3 Shared RAM Features

Using the memory modules supporting a 128-bit data path, the 68040 processor can read and write a complete cache line in one transaction, thus dramatically improving the performance.
The start and end VMEbus access addresses to the shared RAM are programmable in 4 Kbyte increments via the FGA-002. The defined memory range can be write-protected in combination with the address modifier codes. For example, the FGA-002 may be programmed so that, in supervisor mode, the memory may be read or written from the VMEbus while, in user mode, it may only be read. The read/write protection mechanism is fully under the user's software control.
During VMEbus slave accesses to the shared RAM, the FGA-002 can release the local bus early while completing the VMEbus cycle asynchronously. This early completion of VMEbus read/write cycles effectively halves the overhead to the microprocessor for an external access.

1.3 The Cycle Control Chip

In order to enable existing 68020/68030 software to run in the 68040 environment, a Cycle Control Chip (CCC) is integrated on the CPU-40 and CPU-41. It translates the dynamic bus sizing of the 68020 and 68030 microprocessors into allowed and supported 68040 bus cycles.
Additionally, the CCC allows the single 8-bit wide SRAM and EPROM to be accessed as 32-bit wide contiguous memory by the 68040. Furthermore, the CCC handles accesses to the I/O devices and preserves I/O software drivers written for the 68020 or 68030 microprocessors. Since the 68040 is only able to access I/O devices in increments of 4 bytes, the CCC has been designed to allow I/O devices to reside on a 1 or 2 byte boundary but still be compatible with the 68040. This feature ensures full software upward compatibility with 68020 or 68030 based board designs from FORCE COMPUTERS.

1.4 The DMA Controller

Incorporated within the FGA-002 is a 32-bit DMA controller which allows DMA transfer between local resources and/or the VMEbus without any degradation in performance of the local microprocessor.
The DMA-controller runs fully independently of the 68040 microprocessor and is able to perform transfers to/from the shared RAM, to/from the VMEbus, to/from local devices and to/from the EAGLE modules connected to the FLXibus.
To increase data throughput, the DMA controller operates using a 32-byte FIFO for internal data storage. The read and write operations are executed in bursts of eight cycles, four bytes at a time. The result is that only eight read cycles followed by eight write cycles are required to transfer 32 bytes of data, even if the source/destination devices are byte oriented.
The 32-byte FIFO as well as the parallel architecture of the CPU-40 and CPU-41 enable the microprocessor to operate in parallel with the DMA controller during data transfers. For example, during VMEbus DMA transfers, the microprocessor can access all local I/O devices, the EPROM area and the shared RAM without any performance degradation. In addition, the DMA controller is connected to the FLXibus, allowing fast data transfers between EAGLE modules and the shared RAM or VMEbus memory.

The DMA controller adapts to both aligned and unaligned data transfers. The internal control logic automatically aligns the data to take full advantage of the 32-bit structure of the VMEbus and the shared RAM.

1.5 The EAGLE Module Interface

The EAGLE module interface consists of the FORCE Local eXpansion interface bus (FLXibus) and the EAGLE I/O interface. Incorporated on the CPU-40 and CPU-41, the EAGLE module interface allows the user to expand the I/O functionality of the base boards via the installation of EAGLE I/O subsystem modules. FORCE COMPUTERS offers a variety of EAGLE modules to suit most standard application requirements. As an open specification, the FLXibus enables the user to easily design customer specific I/O modules, exactly tailored to the target application.

The EAGLE module interface and the EAGLE modules themselves are designed to allow a complete CPU-40/CPU-41 solution to occupy only one VMEbus slot. When installed, the EAGLE module's front panel becomes part of the base board's front panel, completing a mechanically sound and compact product.

1.5.1 The FLXi

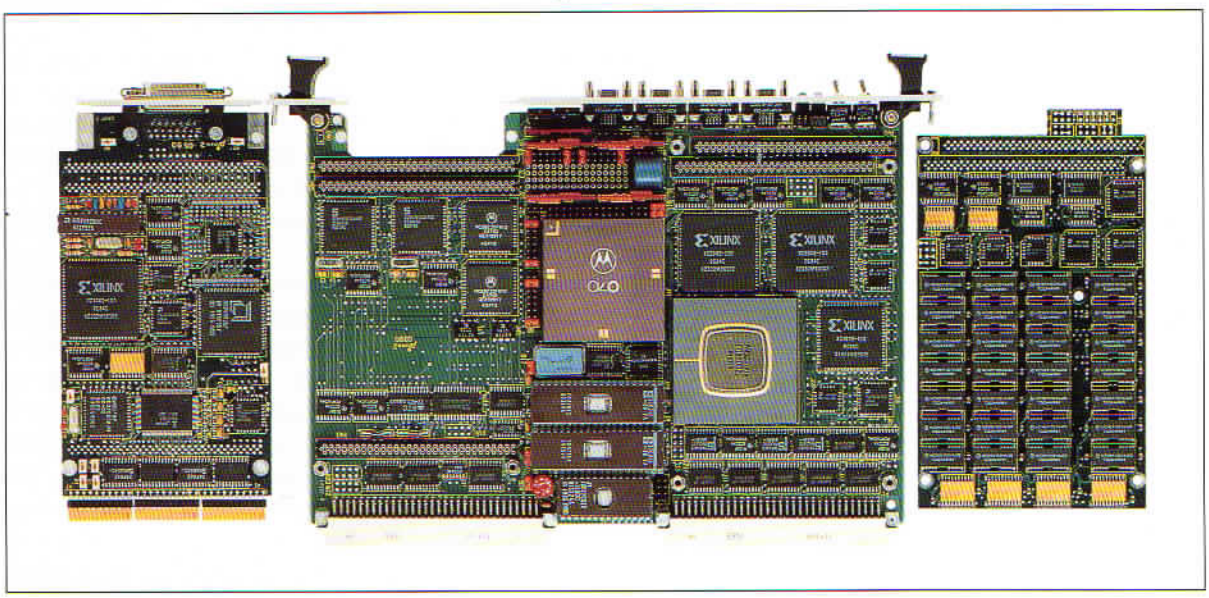
The FLXi supports non-multiplexed 32-bit data and address buses for microprocessor and DMA access using 68020 compatible bus timing and dynamic bus sizing. This provides adequate I/O bandwidth to support the demands of high performance and intelligent I/O subsystems on an EAGLE module.

The FLXibus is master/slave capable, allowing the EAGLE module to access the resources of the base board in addition to the 68040 on the base board being able to access the resources on the EAGLE module. Because of the EAGLE modules' ability to interrupt the base board and vice versa, FLXi supports all types of functions ranging from interrupt intensive I/O to independently intelligent subsystems.

1.5.2 The EAGLE I/O Interface

In addition to the FLXi, a direct connection of the 64 VMEbus P2 user I/O pins (rows A and C) is provided on the EAGLE interface. This enables the EAGLE module's I/O signals to be routed to the front panel, to the VMEbus P2 connector or to both. Depending on the EAGLE module installed, these signals may be, for example, a VSB interface, serial I/O, Ethernet, SCSI and/or floppy I/O or any other application specific interface.

SYS68K/CPU-40 with EAGLE-01 and Memory Module



1.6 The local SRAM

A 128 Kbyte SRAM with on-board battery back-up and/or +5V STDBY from VMEbus is installed on all CPU-40 and CPU-41 board versions. This supports data storage during power down phases for at least one year. The SRAM is directly connected to the I/O interface of the FGA-002.

1.7 The Flash EPROM

A 128 Kbyte Flash EPROM is included on the base board of the CPU-40 and the CPU-41 which can be used as additional data back-up under conditions of power down for long periods. Flash EPROM is also particularly well-suited for storing details of the board status, such as S/W revision, board or system serial numbers, dates of production or revisions and any other board relevant information.

1.8 The System EPROMs

The CPU-40 and the CPU-41 contain two 40-pin EPROM sockets for the installation of two 16-bit wide EPROM devices. The EPROMs operate with a 200 ns access time.The EPROMs present a full 32-bit data path to the processor, allowing much higher performance compared to 8-bit wide implementations.

The following devices are supported in the System EPROM area:

Organization	Total Capacity
64 K x 16	256 Kbyte
128 K x 16	512 Kbyte
256 K x 16	1 Mbyte

1.9 The Boot EPROM

The CPU-40 and the CPU-41 boards contain, in addition to the two system EPROMs, a single boot EPROM to boot the local microprocessor, initialize all I/O devices and program the board dependent functions of the FGA-002. All the basic initialization of the I/O devices and the FGA-002 are made through the Boot EPROM. In addition, the Boot EPROM contains User Utility Routines, which may be called from the user's application program. These routines provide easy software access to the functionality of the FGA-002 (DMA-controller, FORCE Message Broadcast, Interrupt Management etc.).

1.10 The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the CPU-40 and the CPU-41 to provide serial communication to other parts of the user's system.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit or character oriented protocols. With additional software, this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.

All four channels are routed to 9-pin micro D-sub connectors on the front panel. The CPU-40 and the CPU-41 are supplied with all four serial I/O channels connected to RS232 compatible socketed hybrid drivers/receivers. All channels can be individually configured for RS422/485 compatibility simply by exchanging the modules with optionally available hybrids. The DUSCCs can interrupt the local microprocessor on a software programmable level (1 to 7).
To support synchronous communication, a jumper field is provided to allow the user to connect TxClk and RxClk to the 9-pin connectors.
An adapter cable is provided with the CPU-40 and the CPU-41 to allow connection of standard 9-pin D-sub connectors to the 9-pin micro D-sub connectors.

1.11 The Real-Time Clock

A software programmable Real Time Clock (RTC-72423) with on-board battery back-up and/or +5V STDBY support from VMEbus is installed on the CPU-40 and the CPU-41 boards. Battery back-up ensures continued operation of the RTC for at least one year after power-down.

Features of the Real-Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- CMOS design provides low power consumption during power-down mode

1.12 The Parallel Port

A 12-bit parallel I/O port is routed to a 24-pin header which allows the connection of a flat cable. Eight bits are connected to port A of a PI/T (Parallel Interface and Timer 68230) device and can be used as inputs or outputs. The remaining four bits are connected to the handshake pins of the PI/T.
This port can be used for parallel I/O applications and, with additional logic, as a Centronics-compatible printer interface.

1.13 The Timers

A total of three independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to interrupt the microprocessor on a software programmable IRQ level (1 to 7).
The first two timers are each 24-bit wide with individual 5-bit prescalers.The third timer can be used to generate interrupts to the microprocessor and the SYSFAIL signal to the VMEbus. It can also be used to act as a watchdog. This is an 8-bit timer with a programmable source clock divider, installed in the FGA-002.
The SYSFAIL signal can be used in multiprocessor systems to signal that one board has detected a failure. It can be asserted if the watchdog timer is not regularly reset. The reset time interval to prevent SYSFAIL is fully software programmable.

2. EAGLE Modules

EAGLE modules are I/O sub-systems designed not only to increase the functionality of the board but to add the exact I/O features to fit the application requirement. EAGLE modules connect directly onto the FLXibus of the base board. FLXibus and EAGLE modules will be a feature on future FORCE board generations to ensure continued compatible flexibility.

2.1 The EAGLE-01

The EAGLE-01 connects to the FLXibus on the CPU-40 and CPU-41. The module provides disk and networking support to complement the features of the base board.

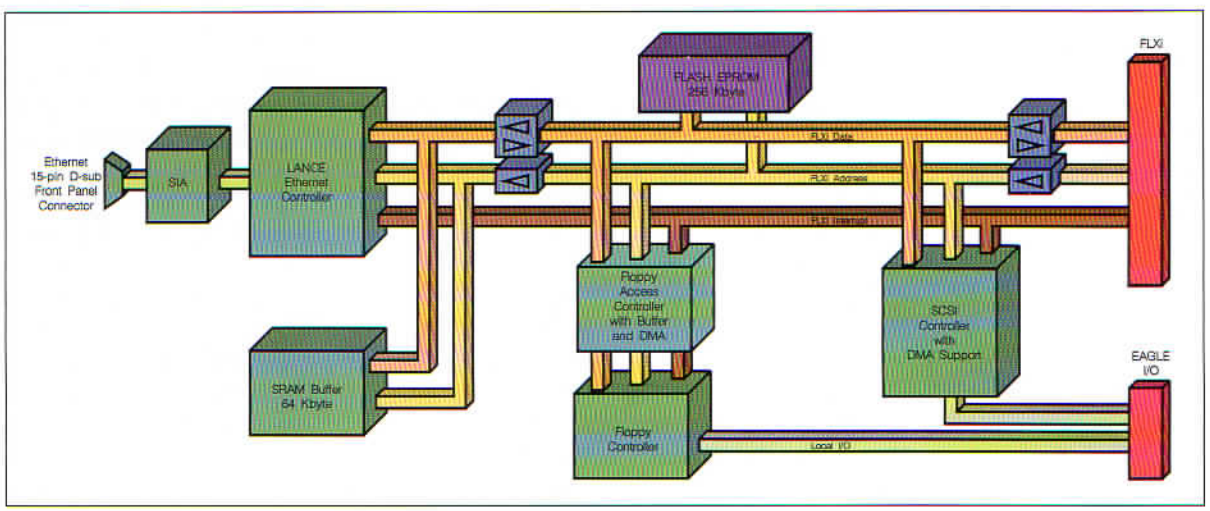
Features of EAGLE-01

- SCSI Controller (87031) connected to the DMA interface of the FGA-002.
- Floppy Disk Controller (37C65) with dedicated 16 Kbyte sector buffer.
- Local Area Network Controller (Am7990) providing a complete Ethernet interface.
- 64 Kbyte SRAM for buffering Ethernet packets.
- 256 Kbyte Flash EPROM for storage of EAGLE-01 firmware and drivers.

2.1.1 The SCSI Interface

The 87031 SCSI controller is included in the EAGLE-01 to interface directly to SCSI Winchester disks, optical disk drives, tape streamers or other SCSI compatible device. The 8-bit DMA

Block diagram of the EAGLE 01



channel of the SCSI controller is connected directly to the DMA controller of the FGA-002. The I/O signals of the single-ended SCSI interface are provided directly on the VMEbus P2 connector of the base board and are fully compatible with the pin assignment of the SYS68K/IOBP-1 and IOPI-2 Input/Output Back Panels simplifying interconnection to mass memory devices.

Features of the 87031 SCSI Controller

- Full support for SCSI control
- Service of initiator or (with user-supplied software) target device
- 8-byte data buffer register
- Transfer byte counter (24-bit)
- Independent control and data transfer bus

2.1.2 The Floppy Disk Interface

The 37C65 device installed on the EAGLE-01 provides the interface between the CPU-40/CPU-41 and a floppy disk drive. The module incorporates a buffer memory and a DMA controller to ensure maximum performance and minimum degradation of the real-time responsiveness of the board at all times. A DMA controller is included on the EAGLE-01 to perform DMA transfers between the 37C65 and the 16 Kbyte sector buffer memory. Data is transferred between the sector buffer and the base board through the FGA-002's DMA controller. This architecture allows the microprocessor to function at full performance while slower floppy disk transfers can take place in parallel.
The floppy disk controller fully supports double density and high density floppy media for one or two 3½" and 5¼" drives.
The floppy interface is routed to the P2 connector of the base board and is fully compatible with the SYS68K/IOBP-1 and IOPI-2 interconnection pin assignment.

2.1.3 The Ethernet Controller

The Am7990 (LANCE) chip set provides conformance to the IEEE 802.3 Ethernet interface standard. This allows, with additional software, the support of higher level Local Area Network (LAN) communication protocols.

Features of the Am7990 (LANCE)

- Compatible with IEEE 802.3 Rev.0
- On-chip DMA and buffer management
- 48-byte FIFO
- 24-bit linear addressing
- Network and packet error reporting
- Back-to-back reception with as little as 4.1 microsecond inter-packet gap time
- Diagnostic routines

The LAN interface on the EAGLE-01 uses a design that ensures that the microprocessor and the Ethernet controller can operate in parallel, maintaining the full real-time capability of the board in an Ethernet environment.
This architecture includes a dedicated 64 Kbyte buffer memory for Ethernet data transfers. This buffer is a dual ported memory array, allowing access from both the Am7990 and from the local 68040 through FLXi. This 64 Kbyte buffer stores outgoing or incoming data packets until either the system is ready to allow data transmission from the CPU node or the CPU is ready to process the incoming data.
An incoming data packet is transferred to the buffer memory under control of the DMA controller contained within the Am7990. Arrival of the data is flagged via an interrupt to the 68040 and the application software determines when the packet should be transferred from the buffer memory. This transfer is then performed by the DMA controller inside the FGA-002.
An outgoing packet is transferred into the buffer memory by the FGA-002 DMA controller. The Am7990 DMA controller then transfers the data out again when it is ready to transmit onto the network.
The Ethernet interface is provided by a standard 15-pin D-sub transceiver connector mounted on the front panel of the EAGLE-01.

2.1.4 The Flash EPROM

A 256 Kbyte Flash EPROM area is installed on the EAGLE-01 module reserved for the user's applications. Flash EPROM ensures easy maintenance and update of software since code can be erased and re-programmed while the board remains installed in the system. It is even possible to change or load code remotely via a network or even a telephone line, eliminating the need for costly down-time or service visits. For security, the FLASH EPROM on the EAGLE-01 can be write protected via a switch.

2.1.5 The Parallel Architecture

The parallel architecture of the CPU-40 and the CPU-41 together with the EAGLE-01 ensures the maintenance of full real-time capability, even if numerous I/O transfers have to be performed while the microprocessor fulfils number crunching tasks. This is achieved by implementing different independent data transfer paths with dedicated DMA support on the single board system. For example, DMA transfers to/from floppy disk, Ethernet or SCSI are fully asynchronous and independent of each other. This guarantees that full real-time responsiveness of the 68040 is maintained.

The following table shows the 68040 performance during DMA transfers with an EAGLE-01 installed:

Transfer to/from	Transfer from/to	CPU performance
VMEbus	SCSI	100%
VMEbus	Floppy Disk Buffer	>80%
VMEbus	Ethernet Buffer	>65%
Shared RAM	SCSI	>90%
Shared RAM	Floppy Disk Buffer	>80%
Shared RAM	Ethernet Buffer	>65%

2.2 Additional EAGLE Modules

The flexible architecture of the CPU-40 and the CPU-41 also allows the installation of other EAGLE modules on the FLXibus. A continually increasing number of standard EAGLE modules is available from FORCE COMPUTERS and third parties to offer various I/O options such as VSB interface (EAGLE-02), high speed serial I/O (EAGLE-03, EAGLE-18) or GPIB/IEEE488 (EAGLE-19).
However, the EAGLE module concept is intended to adapt any FORCE board incorporating the FORCE Local eXpansion interface to the particular application environment. In order to shorten design times of EAGLE modules, and to allow easier customer EAGLE module development, FORCE COMPUTERS has designed a custom device, the FC68165, to interface directly between the FLXibus and module based I/O devices.

3. The Memory Map

Start Address	End Address	Type
00000000	00FFFFFF	Shared Memory (16 Mbyte)
01000000	F9FFFFFF	VMEbus Addresses (16 Mbyte) A32: D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus A24: D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus A16: D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus A24: D16, D8
FCFF0000	FCFFFFFF	VMEbus A16: D16, D8
FD000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	System-EPROM
FF800000	FFBFFFFF	Local I/O
FF800C00	FF800DFF	PI/T 1
FF800E00	FF800FFF	PI/T 2
FF802000	FF8021FF	DUSCC 1
FF802200	FF8023FF	DUSCC 2
FF803000	FF8031FF	RTC-1
FFC00000	FFC7FFFF	LOCAL SRAM
FFC80000	FFCFFFFF	LOCAL FLASH EPROM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	BOOT EPROM
FFF00000	FFFFFFFF	Reserved

4. The VMEbus Interface

The CPU-40 and the CPU-41 include a full 32-bit VMEbus interface. The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode. In slave mode, the address modifiers for A32 and A24 are fully supported.
Read-Modify-Write cycles are fully supported to allow multiple CPU boards to be synchronized via the shared RAM. The FGA-002 determines whether or not an access to the shared RAM is allowed and, if allowed, controls the access cycle.

The CPU-40 and the CPU-41 provide an interrupt handler capability (IH 1-7) which can be enabled/disabled under software control. The CPU-40 and the CPU-41 also provide a VMEbus interrupter function that allows the board to send interrupts on one of 7 programmable levels with a software programmable vector.

When the CPU-40 or CPU-41 is VMEbus master, the following bus release modes are supported:

RWD	=	Release When Done
ROR	=	Release On Request
RBCLR	=	Release On Bus Clear
RAT	=	Release After Timeout
REC	=	Release Every Cycle
ROACF	=	Release on ACFAIL

Each release mode is software programmable inside the FGA-002. The bus request level of the CPU-40 and CPU-41 is jumper selectable (BR0-3) or software programmable.
The DMA controller in the FGA-002 on the CPU-40 and CPU-41 is able to access the VMEbus interface independently from the microprocessor, enabling VMEbus communication to take place without impacting the processing capabilities of the rest of the board for number crunching or servicing on-board I/O.
A four-level VMEbus arbiter with prioritized, round robin and prioritized round robin arbitration modes; a power monitor; a SYSRESET generator; IACK driver and support for ACFAIL, SYSFAIL and SYSCLK complete the VMEbus interface.

5. The Interrupt Structure

The FGA-002 installed on the CPU-40 and CPU-41 handles all local and VMEbus interrupts. All interrupt requests from the local bus are combined with the seven VMEbus IRQs. Interrupts from the FLXibus are also channelled through the FGA-002.
The FGA-002 can be programmed by the user to prioritize interrupts from any source and then to interrupt the 68040 on any interrupt level (1 to 7). The FGA-002 supplies the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus, depending on the programmed configuration of the FGA-002. This process is fully under the control of the application software.

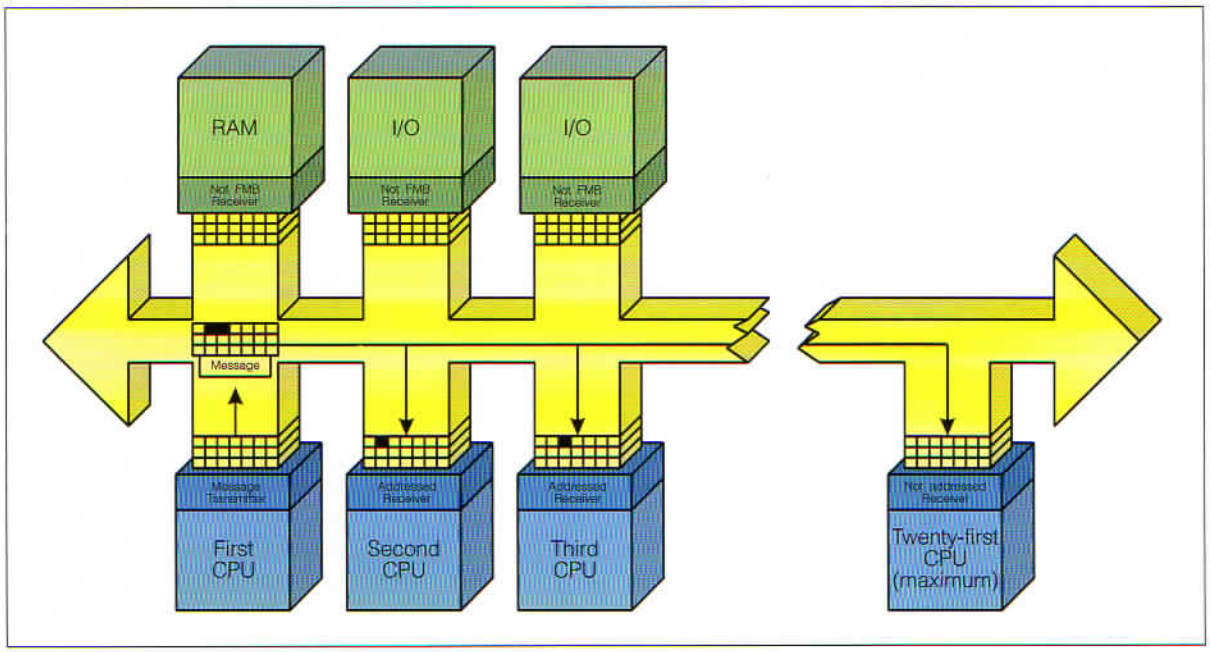
6. The Multiprocessor Mailboxes

The CPU-40 and the CPU-41 include eight multiprocessor mailboxes. Each of these allows an interrupt to be generated to the local 68040 microprocessor by another VMEbus board. The interrupt level of each multiprocessor mailbox is software programmable and an individual interrupt vector for each mailbox may be passed to the microprocessor.
This function allows triggering an interrupt on the CPU-40 or the CPU-41 from multiple masters on the VMEbus. The mailboxes are accessed via RMW access, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

7. FORCE Message Broadcast

All FORCE VME/PLUS boards provide two fully independent message broadcast channels which are implemented within the FGA-002. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message, making it especially well suited for high priority messages.
The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multiprocessing systems based on the VMEbus.
An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 specification. Any 32-bit VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.
All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system.
The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multiprocessor environments. Without the FMB mechanism, communication between and synchronization of system boards has to be managed via the seven interrupt request lines. FMB reduces the time overhead normally needed to process the interrupt cycles to just one write cycle.

Block Diagram of the FORCE Message Broadcast (FMB)



8. The I/O Back Panels

To simplify connection of its single board computers within system environments, FORCE COMPUTERS also offers the SYS68K/IOBP-1 and IOPI-2 backpanels which split the pins of the P2 connector of the VMEbus backplane into 2 cables with industry standard connectors. The SYS68K/IOBP-1 and IOPI-2 are compatible with the pin-out of all FORCE CPU cards.
SYS68K/IOBP-1 and IOPI-2 directly connect to the I/O pins of the P2 connector of the VMEbus backplane and route them to connectors for two flat ribbon cables. The first connector interfaces to a standard SCSI flat cable with full support for the ground shield. The second is used to interface directly to floppy disk drive(s), and also fully supports the ground shield.

9. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or a third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-40 and CPU-41 Software Support

Operating System / Kernel	Vendor / Support
VxWORKS	FORCE COMPUTERS/ WIND RIVER SYSTEMS
OS-9	FORCE COMPUTERS/ MICROWARE
PDOS	EYRING
VMEPROM	FORCE COMPUTERS
VRTX-32	READY SYSTEMS
pSOS+	INTEGRATED SYSTEMS (SOFTWARE COMPONENTS GROUP)

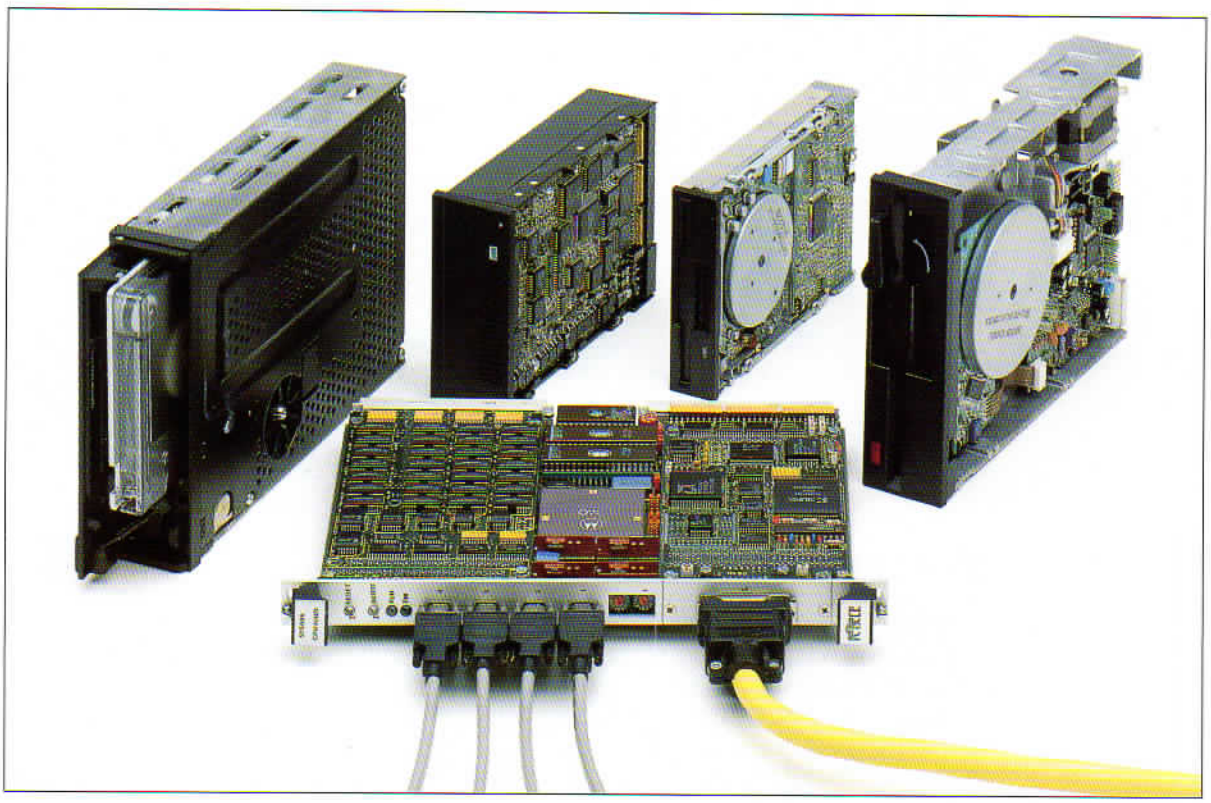
As an added bonus, FORCE COMPUTERS provides the user with the ability to immediately start a real-time application by including VMPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is a real-time multitasking kernel/monitor. The complete package uses 256 Kbyte of EPROM space and 32 Kbyte of RAM for system variables and 260 Kbyte for hashing buffers on top of the RAM area. VMEPROM fully supports

all of the on-board I/O devices. VMEPROM is composed of a highly sophisticated real-time kernel, based on PDOS version 3.3. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

- Real-Time Kernel supporting multitasking, up to 64 tasks.
- File manager, supporting up to 64 open files at the same time.
- Line assembler/disassembler with full support of all 680x0 instructions.
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify.
- S-record up/downloading from any port defined in the system.
- Disk support for RAM disk, floppy and Winchester disks.
  VMEPROM allows disk formatting and initialization.
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system.
  Local serial I/O devices are also supported.
- EPROM programming utility using the SYS68K/RR-2 board.
- Full screen editor.
- I/O re-direction to files or ports from the command line.
- Over 100 system calls to the kernel.

SYS68K/CPU-40 and Mass Memory Devices



Specifications

Function		
CPU type		68040
CPU clock frequency on:	CPU-40B/x, CPU-41B/x	25.0 MHz
Shared DRAM capacity with parity	CPU-40B/4 CPU-40B/16 CPU-40B/32	4 Mbyte 16 Mbyte 32 Mbyte
Shared SRAM capacity	CPU-41B/4 CPU-41B/8	4 Mbyte 8 Mbyte
SRAM capacity with on-board battery back-up		128 Kbyte
Number of system EPROM sockets Data path		2 32-bit
Serial I/O interfaces (68562) RS232/422/485 compatible		4 4 of 4
24-bit timer with 5-bit prescaler 8-bit timer		2 1
Parallel I/O interface (68230) Real Time Clock with on-board battery back-up (72423)		12 lines yes
VMEbus interface	A32, A24, A16 : D8, D16, D32, UAT, RMW A32, A24 : D8, D16, D32, RMW	Master Slave
SYSCLK driver Mailbox interrupts		yes 8
FORCE Message Broadcast	FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus and local interrupt handler All sources support programmable IRQ level		1 to 7 yes
RESET/ABORT Switches		yes
Firmware installed		VMEPROM FGA-002 Boot EPROM
Power requirements	+ 5V max for CPU-40 + 5V max for CPU-41 +12V max −12V max	6.0 A 5.0 A 0.3 A 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing in %)		0°C to +50°C −40°C to +85°C 0 to 95
Board dimensions		234 x 160 mm : 9.2 x 6.3 in (6U)
Number of slots used		1

EAGLE-01 Specifications

Number of slots when used with CPU-40 or CPU-41	1
Ethernet interface on EAGLE-01 Ethernet SRAM	Am7990 64 Kbyte
SCSI Interface (87031) on EAGLE-01	Single-ended
Floppy Disk Interface (37C65) on EAGLE-01	SA 460

Ordering Information

SYS68K/CPU-40B/4-00 Part No. 102000	25.0 MHz 68040 based CPU board with DMA, 4 Mbyte shared DRAM, 4 serial I/O channels, FLXibus, VMEPROM. Documentation included.
SYS68K/CPU-40B/4-01 Part No. 102001	25.0 MHz 68040 based CPU board with DMA, 4 Mbyte shared DRAM, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-40B/16-00 Part No. 102100	25.0 MHz 68040 based CPU board with DMA, 16 Mbyte shared DRAM, 4 serial I/O channels, FLXibus, VMEPROM. Documentation included.
SYS68K/CPU-40B/16-01 Part No. 102101	25.0 MHz 68040 based CPU board with DMA, 16 Mbyte shared DRAM, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-40B/32-00 Part No. 102104	25.0 MHz 68040 based CPU board with DMA, 32 Mbyte shared DRAM, 4 serial I/O channels, FLXibus, VMEPROM. Documentation included.
SYS68K/CPU-40B/32-01 Part No. 102105	25.0 MHz 68040 based CPU board with DMA, 32 Mbyte shared DRAM, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-41B/4-00 Part No. 103000	25.0 MHz 68040 based CPU board with DMA, 4 Mbyte shared SRAM, 4 serial I/O channels, FLXibus, VMEPROM. Documentation included.
SYS68K/CPU-41B/4-01 Part No. 103001	25.0 MHz 68040 based CPU board with DMA, 4 Mbyte shared SRAM, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-41B/8-00 Part No. 103002	25.0 MHz 68040 based CPU board with DMA, 8 Mbyte shared SRAM, 4 serial I/O channels, FLXibus, VMEPROM. Documentation included.
SYS68K/CPU-41B/8-01 Part No. 103003	25.0 MHz 68040 based CPU board with DMA, 8 Mbyte shared SRAM, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 700043	Back panel for single board computers providing SCSI and floppy disk drive connectors.
IOPI-2 Part No. 510327	Back panel for single board computers providing SCSI and floppy disk drive connectors.
SYS68K/CABLE MICRO-9 SET 1 Part No. 700101	Set of three adapter cables 9-pin micro D-sub male connector to 9-pin D-sub female connector, length 2 m.
SYS68K/CABLE MICRO-9 SET 2 Part No. 700102	Set of four adapter cables 9-pin micro D-sub male connector to 25-pin D-sub female connector, length 2 m.
SYS68K/CPU-40/UM Part No. 800300	User's manual for the SYS68K/CPU-40 including VMEPROM and FGA-002 user's manual.

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